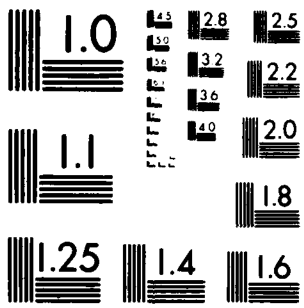
AD-A108 016 VARIAN ASSOCIATES INC PALO ALTO CA SOLID STATE LAB F/G 9/1
RESEARCH ON INGAAS FETS.(U)
SEP 81 R YEATS, K VON DESSONNECK, S BANDY N00014-78-C-0380

UNCLASSIFIED NL

END
DATE FILMED
1 82
DTIC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

LEVEL III

(12)

A090141

AD A108016

FINAL REPORT

Research on InGaAs FETs

September 1981

Prepared by:

R. Yeats, K. Von Dessonneck, S. Bandy and Y. Chai

VARIAN ASSOCIATES, INC.
Solid State Laboratory
611 Hansen Way
Palo Alto, CA 94303

This research was sponsored by the Office of
Naval Research under Contract No. N00014-78-C-0380.
Contract Authority: NR 251-030

18

TABLE OF CONTENTS

UNCLASSIFIED 16 RF54581

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER Final Report	2. GOVT ACCESSION NO. AD A108016	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) 6 Research on InGaAs FETs.	9	5. TYPE OF REPORT & PERIOD COVERED Final Report. May 1978 — August 1981 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) 1 R. Yeats, K. Von Dessonneck, S. Bandy and Y. G. Chai	15	8. CONTRACT OR GRANT NUMBER(s) N00014-78-C-0380
9. PERFORMING ORGANIZATION NAME AND ADDRESS Varian Associates, Inc. 611 Hansen Way Palo Alto, CA 94303	17	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS PE-62762N RF-54-581-001 NR 251-030
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research 800 N. Quincy Street Arlington, VA 22217	11	12. REPORT DATE September 1981 13. NUMBER OF PAGES 35
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) 12 37		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

Reproduction in whole or in part is permitted for any purpose of the United States Government.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

p-n junction FET
InGaAs epitaxial growth
JFET
InGaAs FET
$In_{.53}Ga_{.47}As$

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A process has been established for fabricating $In_{.53}Ga_{.47}As$ JFETs on InP substrates that is capable of making JFETs with small gate lengths (≈0.5 μm), low source resistance (2Ω), low gate series resistance (<4Ω), negligible "side-wall" capacitance, and low gate leakage current (≲100 nA). The process involves a shallow localized Zn diffusion and a controlled etch using the gate metal as a mask. The effective gate length is somewhat smaller than the gate metal "length", thus facilitating the formation of submicron gates.

DD FORM 1473, 1 JAN 73 EDITION OF 1 NOV 65 IS OBSOLETE

409110

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

At modest reverse-bias gate voltages, these JFETs have g_m values approaching twice that which would be expected for corresponding GaAs MESFETs. However, near zero-gate bias, there is substantial g_m compression, perhaps arising from defects associated with the Zn-diffusion process. Further device optimization is still required along the lines of increasing channel doping, decreasing gate length, and developing improved diffusion processes (e.g., ion-implantation). Optimized $In_{.53}Ga_{.47}As$ JFETs will probably outperform even the best GaAs MESFETs.

SUMMARY

omega

A process has been established for fabricating $In_{.53}Ga_{.47}As$ JFETs on InP substrates that is capable of making JFETs with small gate lengths ($\approx 0.5\ \mu m$), low source resistance ($2\ \Omega$), low gate series resistance ($< 4\ \Omega$), negligible "sidewall" capacitance, and low gate leakage current ($\lesssim 100$ nA). The process involves a shallow localized Zn diffusion and a controlled etch using the gate metal as a mask. The effective gate length is somewhat smaller than the gate metal "length", thus facilitating the formation of submicron gates. At modest reverse-bias gate voltages, these JFETs have g_m values approaching twice that which would be expected for corresponding GaAs MESFETs. However, near zero-gate bias, there is substantial g_m compression, perhaps arising from defects associated with the Zn-diffusion process. Further device optimization is still required along the lines of increasing channel doping, decreasing gate length, and developing improved diffusion processes (e.g., ion-implantation). Optimized $In_{.53}Ga_{.47}As$ JFETs will probably outperform even the best GaAs MESFETs.

I. INTRODUCTION

1.1 Motivation for Development of $In_xGa_{1-x}As$ FETs

In recent years, there has been increased interest in $In_xGa_{1-x}As$ FETs. This interest arises from certain material properties of $In_xGa_{1-x}As$ that are expected to lead to favorable device properties, as compared to GaAs FETs. $In_xGa_{1-x}As$ has a lower bandgap than GaAs. This leads to a smaller effective mass for electrons, which in turn leads to higher electron mobility (μ) and tends to lead to a larger value for the saturated drift velocity (v_s). While the higher mobility helps to reduce parasitic resistance, the larger value for v_s is more important, in that the transconductance (g_m) and the speed of the FET are proportional to v_s.

In addition to its smaller bandgap, $In_xGa_{1-x}As$ has a greater energy separation between the nearest conduction band satellite valley (L) and the central valley minimum (Γ). This tends to reduce intervalley electron transfer, which also helps to increase v_s and in addition tends to decrease Gunn-effect current instabilities. Reduction of such instabilities should result in lower noise FETs. Noise will also be reduced by the larger values of g_m that are expected to occur for the increased v_s.

1.2 Previous Results

This is the final report for this contract. $In_xGa_{1-x}As$ FETs have been fabricated in earlier work under this contract (N00014-78-C-0380), and have been described in previous contract reports.[1,2] These efforts met with limited success and will now be summarized. Initially, $In_xGa_{1-x}As$ FETs with x = 0.33-0.34 were grown by vapor phase epitaxy (VPE) on GaAs substrates. Such FETs were somewhat difficult to grow due to the lattice mismatch between the epilayer and the substrate. These

FETs were found to have $v_s = 1.8 \times 10^7$ cm/sec, which is 40% larger than for GaAs FETs. Nevertheless, they were relatively noisy, having noise figures of ≈ 3.2 dB at 8 GHz with an associated gain of $G_a = 14.2$ dB. The poor noise performance resulted from the use of an n^+ substrate. Attempts to grow high-quality VPE layers on semi-insulating GaAs substrates were not successful.

In an effort to improve performance, structures having no lattice mismatch were fabricated. This is accomplished by growing $In_{.53}Ga_{.47}As$ on InP substrates. This particular composition of $In_xGa_{1-x}As$ has the same lattice constant as InP and has a bandgap of 0.75 eV. However, Schottky barriers on $In_{.53}Ga_{.47}As$ are near-shorts, due to the low bandgap. Hence in order to fabricate MESFETs, two modified structures were employed: n-$In_xGa_{1-x}As_yP_{1-y}$/n-$In_{.53}Ga_{.47}As$/S.I.-InP (substrate) and n-InP/n-$In_{.53}Ga_{.47}As$/S.I.-InP (substrate). These structures have a thin high-bandgap lattice-matched layer grown over the $In_{.53}Ga_{.47}As$ layer to facilitate formation of low-leakage Schottky barriers.

The first structure above was grown by liquid phase epitaxy (LPE). The high-bandgap (1.27 eV) InGaAsP layer is used rather than InP to minimize meltback of the $In_{.53}Ga_{.47}As$ layer by the melt for the top layer. MESFETs having this structure were found[2,3] to have $v_s = 2.95 \times 10^7$ cm/sec -- more than twice the value for GaAs, and similar to a recently- reported value[4] of 2.6×10^7 cm/sec for electrons in p-type $In_{.53}Ga_{.47}As$. However, the devices had very poor gain (G = 2 dB) and noise figure (18 dB) at 8 GHz, mainly due to the excessive thickness of the channel. The channel thickness was larger than the gate length which leads to unusually high output conductance.[12] The second structure described above was grown by VPE, which tends to produce slightly lower mobility than LPE. These FETs were also noisy, having a noise figure of 9.5 dB at 8 GHz with about 6 dB associated gain.

1.3 Recent Results

In the most recent work under this contract (described in detail in this report), we have undertaken the fabrication of $In_{.53}Ga_{.47}As$ p-n junction FETs (JFETs). A fabrication process has been established that is capable of making JFETs with small gate lengths (~0.5 μm), low gate series resistance (< 4 Ω), negligible "sidewall" capacitance, and low gate leakage current ($\lesssim$ 100 nA). The process involves a shallow localized Zn diffusion and a controlled etch using the gate metal as a mask. The effective gate length is somewhat smaller than the gate metal "length", thus enabling submicron gates to be more readily obtained.

In order to simplify the development of the process, however, a relatively large gate length mask (1.5 μm) has been employed. Lattice-matched $In_{.53}Ga_{.47}As$ FET layers with $N = 2\text{-}3 \times 10^{16} cm^{-3}$ were grown by MBE on semi-insulating InP substrates. JFETs with gate metallization 300 μm wide and 1.5 μm long have had (external) g_m values of 28 mS, gate series resistance (metal + contact) less than 4 Ω, gate leakage current near pinchoff (2.5V) as low as 20 nA, and source series resistance as low as 2 Ω. Having established the basic processes, improved JFETs could now be fabricated by using more highly doped $In_{.53}Ga_{.47}As$ ($n \approx 9 \times 10^{16} cm^{-3}$) and by using a ≈ 0.5 μm gate mask. It is hoped that such changes will allow the factor of 2 increase in g_m (and speed) that is theoretically expected compared to GaAs MESFETs.

2. $In_{.53}Ga_{.47}As$ MATERIAL GROWTH

Lattice-matched $In_{.53}Ga_{.47}As$ was grown on (100)-oriented Fe-doped InP substrates. Substrates were chemo-mechanically polished using the standard sodium hypochlorite solution and etched in $4H_2SO_4:1H_2O_2:1H_2O$ solution prior to growth. The substrate was mounted on a Mo heater block using In as a bonder and heat-cleaned in the growth chamber at 510°C for 5 minutes. To reduce surface degradation due to preferential evaporation of phosphorus from the substrate, an As_4 over pressure was provided during the cleaning when the substrate temperature reached 300°C. The growth was initiated by opening the shutters interposed between the substrate and the furnaces containing the In, Ga, and As charges. The temperatures of the In and Ga furnaces had been calibrated so that the $In_{.53}Ga_{.47}As$ layer had the same lattice constant as the InP substrate. The Si furnace temperature was set to obtain a free electron concentration of 2-3 x $10^{16}cm^{-3}$. The growth rate used was about 1 μm/hour, and the As_4 to Zn + Ga flux ratio was about 0.8. All the growth was performed at a substrate temperature of 420°C.

MBE layers of $In_{.53}Ga_{.47}As$ with dopings in the mid-$10^{16}cm^{-3}$ range generally have electron mobilities between 5000 and 7000 cm^2/V-sec. Slightly higher mobilities for this doping range are possible by LPE (up to 9000 cm^2/V-sec). MBE $In_{.53}Ga_{.47}As$ layers generally have shiny nearly featureless surfaces, similar to GaAs. There is no sign of strain (i.e., cracks or a cross-hatch pattern).

3. JFET FABRICATION AND RESULTS

3.1 General Background

JFETs have a structure similar to the common Schottky-barrier MESFET. The basic difference is that the gate of a JFET is formed by a p-n junction rather than a Schottky barrier. Schottky barriers heights on $In_{.53}Ga_{.47}As$ are so low and the barriers so leaky that they resemble electrical shorts. On the other hand, $In_{.53}Ga_{.47}As$ p-n junctions can have leakage currents in the 10^{-5} A/cm^2 range[5] at half of the breakdown voltage.

There are two basic JFET structures (Fig. 1). The most commonly seen JFET structure is shown in Fig. 1a. We have chosen not to pursue this structure for several reasons. The minimum gate length for the structure of Fig. 1a is large, about 1 μm. This arises from the ~0.5 μm minimum opening in the SiO_2, and the lateral diffusion of ~0.25 μm on each side, for a junction ~0.25 μm deep (which we shall see is about the smallest acceptable junction depth). Furthermore, the sidewall capacitance arising from the edges of the diffused region is substantial. In fact, the gate "length" entering a capacitance calculation includes the sidewalls and has a minimum value of ~1.5 μm. Another problem with the structure of Fig. 1a is that SiO_2 (and probably SiN_x) are known to be poor passivants for an exposed p-n junction in $In_{.53}Ga_{.47}As$, in that they cause a substantial increase in leakage current.[6,7]

Because of the limitations of the structure of Fig. 1a, we have concentrated our attention on the structure of Fig. 1b. This structure is formed using the gate metal as an etch mask and has negligible sidewall capacitance. Furthermore, the gate length can be smaller than the metallization "length" for favorable etch profiles, thus facilitating the formation of submicron gates.

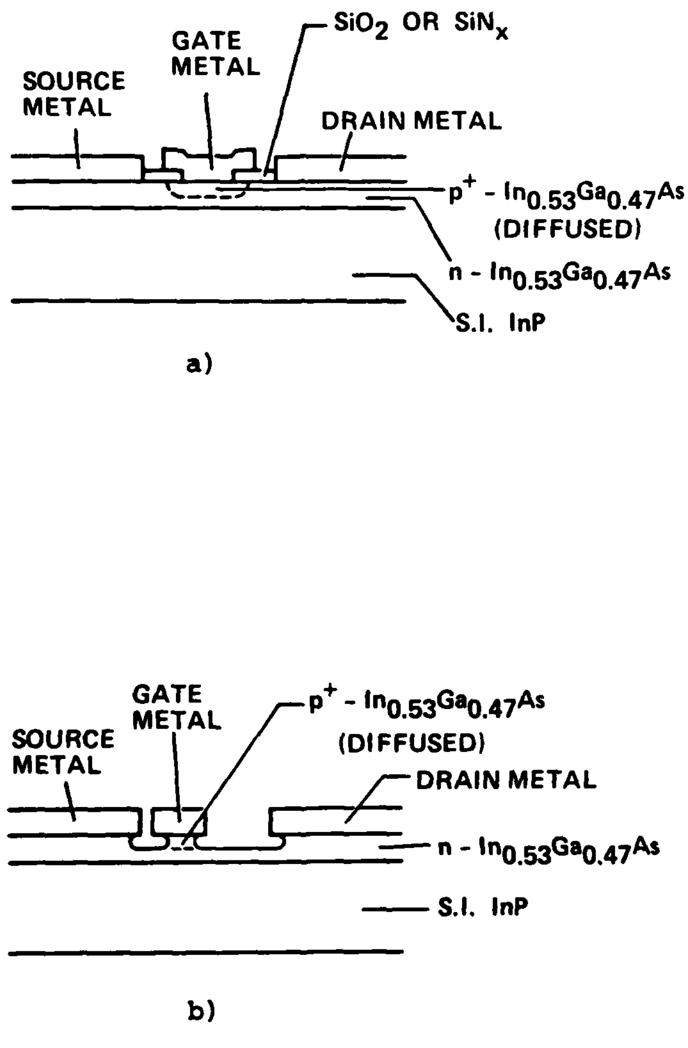


Fig. 1 JFET structures.

A priori, it was not known whether the structure of Fig. 1b would be feasible. Potential problems included:

1) making reproducible shallow diffusions to form high-quality p-n junctions,

2) use of the gate metal as an etch mask (would the resulting metal lips on the gate droop down, thereby shorting out the p-n junction?),

3) obtaining a good etch profile of constant depth across the entire wafer,

4) achieving low gate contact resistance without damaging the underlying shallow p-n junction, and

5) lack of a buffer layer (would the epilayer be damaged by outdiffusion from the Fe-doped substrate or would the substrate interface be of high enough quality to avoid excess leakage, g_m compression, etc.?).

Fortunately, these problems were either minimal or solvable.

3.2 JFET Fabrication Process

We now describe in more detail the JFET fabrication process for the structure of Fig. 1b. First, a layer of lattice-matched $In_{.53}Ga_{.47}As$ is grown by MBE on a (100)-oriented semi-insulating Fe-doped InP substrate. Next, mesas are etched for ~15 sec in a solution of $4H_2O:1HF:1H_2O_2$ using a mask of 1350J photoresist (Fig. 2a). This etch makes extremely flat bevels on all edges of the mesa, thus it is easy to run metal lines over the mesa edges. After removal of the resist, 3000 Å of SiO_2 is deposited and patterned to form openings for Zn diffusion. The Zn

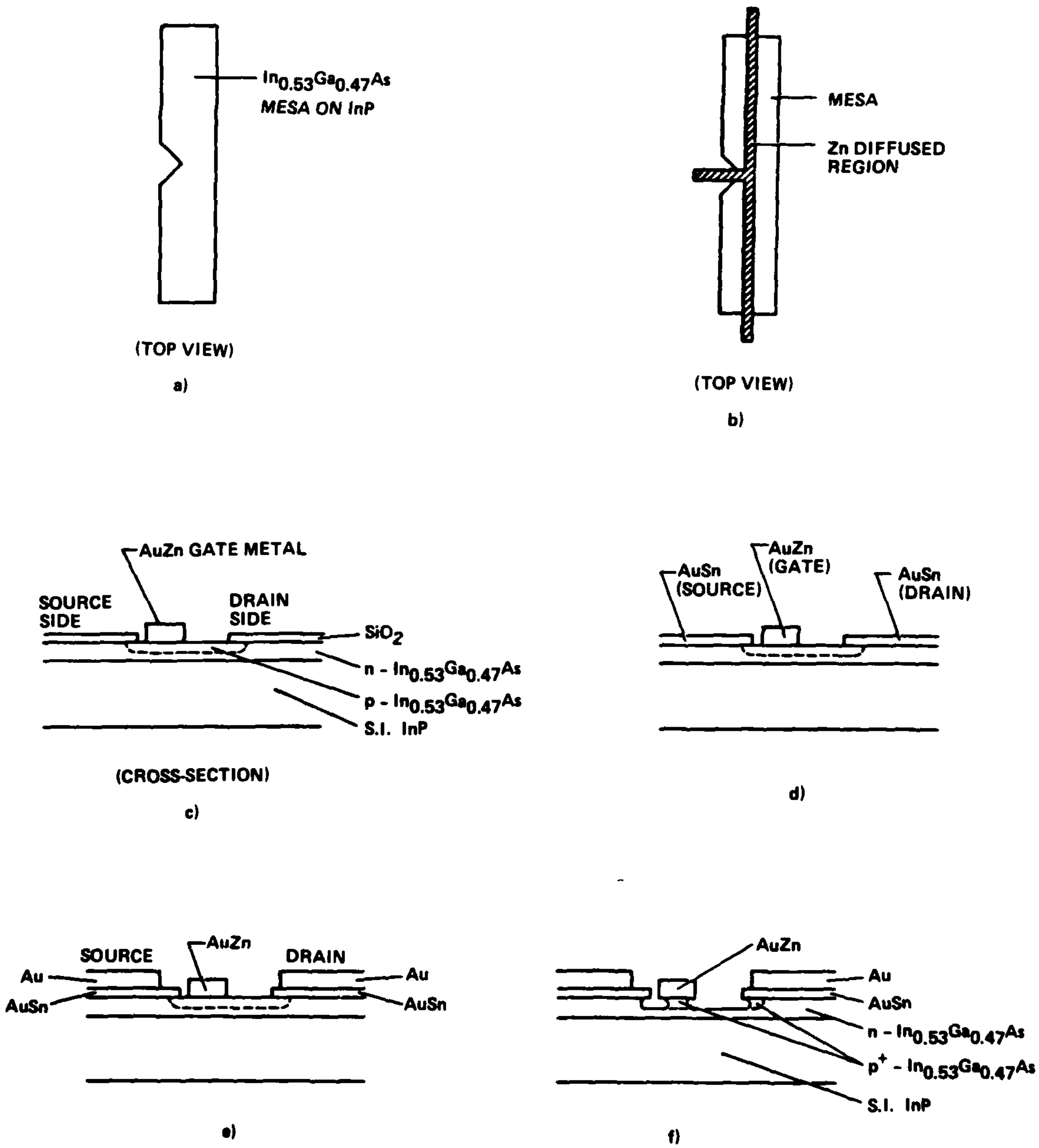


Fig. 2 JFET fabrication process

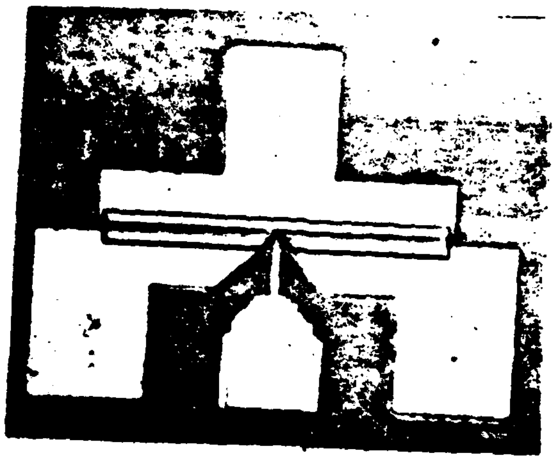


Fig. 2g Completed FET (top view).

diffusion extends beyond the edges of the mesa. This will later keep the gate metal at the edges of the mesa from being shorted to the n-channel (Fig. 2b). The Zn is diffused for ~1 hour at 400°C using an evacuated quartz ampoule containing the wafer and a small quantity of an In-Zn alloy (10 wt.% Zn). Using standard photolithographic liftoff techniques, AuZn gate contact fingers (i.e., gate leads) are formed by e-beam evaporation (Fig. 2c). A typical deposition is 500 Å Au/300 Å Zn/2500 Å Au. We are careful to keep the Zn concentration below the room-temperature solubility of Zn in Au (~15 atomic percent). This is to maximize the electrical conductivity of AuZn by eliminating alloy scattering.

The AuZn gate metallization is located as close as possible to one edge of the SiO_2, which will become the source side of the FET (Fig. 2c). This will reduce the source resistance, thereby improving performance. Next, the SiO_2 is removed and the source/drain contacts are put on by standard techniques (Fig. 2d). These contacts consist of 100 Å Au/200 Å Sn/1000 Å Au deposited by e-beam evaporation. The source is positioned as close to the gate as possible to minimize source resistance. Note that the drain overlaps part of the p-region. This will be helpful in a later step.

Next, the contacts are annealed for 3 min. at 300°C in H_2. Then ~3500 Å of Au is evaporated onto most of the source and drain area, and onto the gate contact pad (Fig. 2e). This is to reduce resistance and to allow wirebonding. Finally, the excess p-region is etched away (Figs. 2f and 2g) using 25 citric acid (50% by weight):$1H_2O_2$ (30% solution), which etches $In_{.53}Ga_{.47}As$ at ~20 Å/sec, which is the same etch rate as for GaAs.[8] The etching is done in small steps. After each step, the gate-drain leakage is examined. Initially, the gate and drain are nearly shorted, since the drain contact overlaps the p-region slightly (Fig. 2d) and since even AuSn forms an ohmic contact to p^{++}-$In_{.53}Ga_{.47}As$.

However, when the etch depth exceeds the depth of the p-n junction, the gate and drain are no longer shorted and instead have a low-leakage p-n junction I-V characteristic. One seeks to etch just barely to the depth of the p-n junction. Further etching thins the external channel region, thereby increasing source and drain resistance and reducing I_{DSS}. On most wafers, the etch depth is uniform across the wafer to better than 400 Å, even for an etch depth of 4000 Å.

The etch profile obtained depends on the orientation of the gate relative to the crystallographic planes. MBE $In_{.53}Ga_{.47}As$ grown on (100)-oriented InP seems to have a slightly granular surface in some regions when observed under very high magnification (1000X). The grains are elongated and parallel to each other and to one of the cleavage planes. Hence these grains can be used to distinguish one cleavage plane (e.g., (011)) from the other $(0\bar{1}1)$. Elongated etch pits can sometimes be formed on thick layers of $In_{.53}Ga_{.47}As$ by etching ~10 minutes with $1NH_2OH:1H_2O_2:2H_2O$. These pits are found to be parallel to the grains. Gates etched in the citric acid/hydrogen perioxide etch that are oriented parallel to the grains have the cross-section shown in Fig. 3a, while those oriented perpendicular to the grains have the cross-section shown in Fig. 3b. The latter is the preferred orientation since the gates are then somewhat shorter than the gate metal length and also have maximum contact area (thus minimizing the contact resistance of the gate metal). Note that the etch leaves fairly flat bottoms. Recently we have experimented with another etch, $1NH_4OH:1H_2O_2:2H_2O$, but have not yet fabricated FETs using it. This etch, which weakens with age, has the cross-section shown in Fig. 4a when the gates are parallel to the grains, and the profile of Fig. 4b when the gates are perpendicular to the grains. (In Fig. 4, the "gate" mask is SiO_2 rather than metal.) Notice the clean flat-bottomed profiles and also that the profile of Fig. 4b will lead to gates that are shorter than the gate metal length.

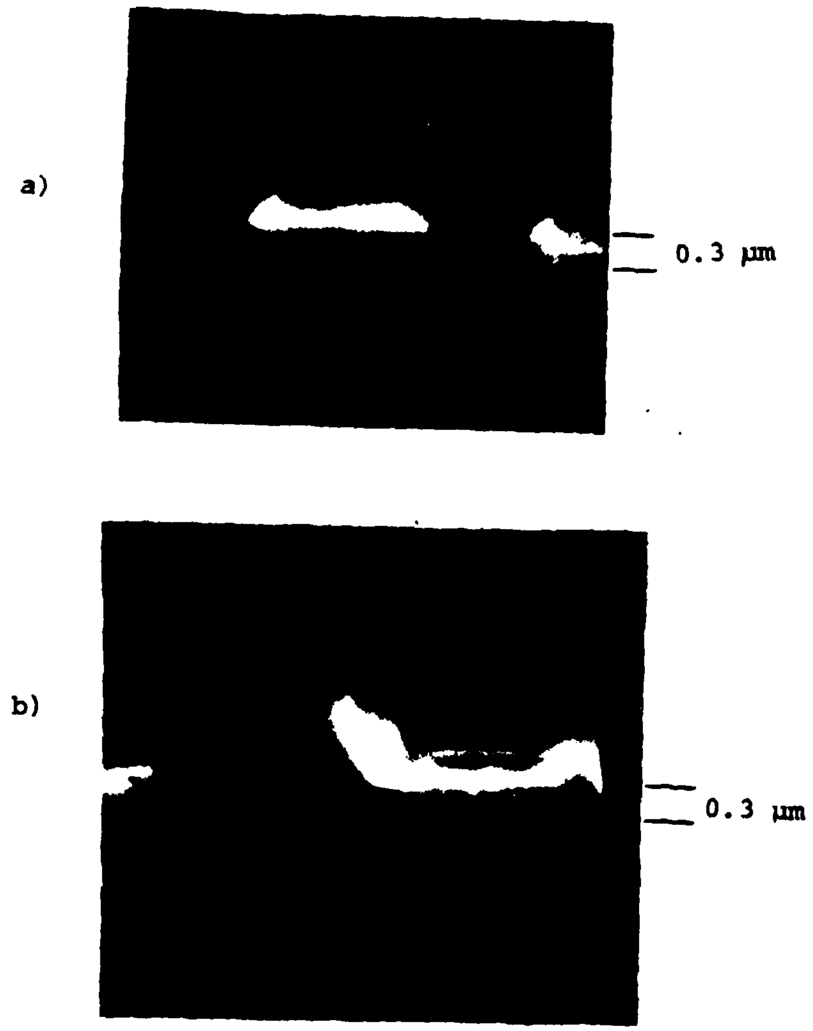


Fig. 3   25 citric acid:1H_2O_2 etch profiles in $In_{.53}Ga_{.47}As$.
(a) cross-section for gates parallel to grains.
(b) cross-section for gates perpendicular to grains.

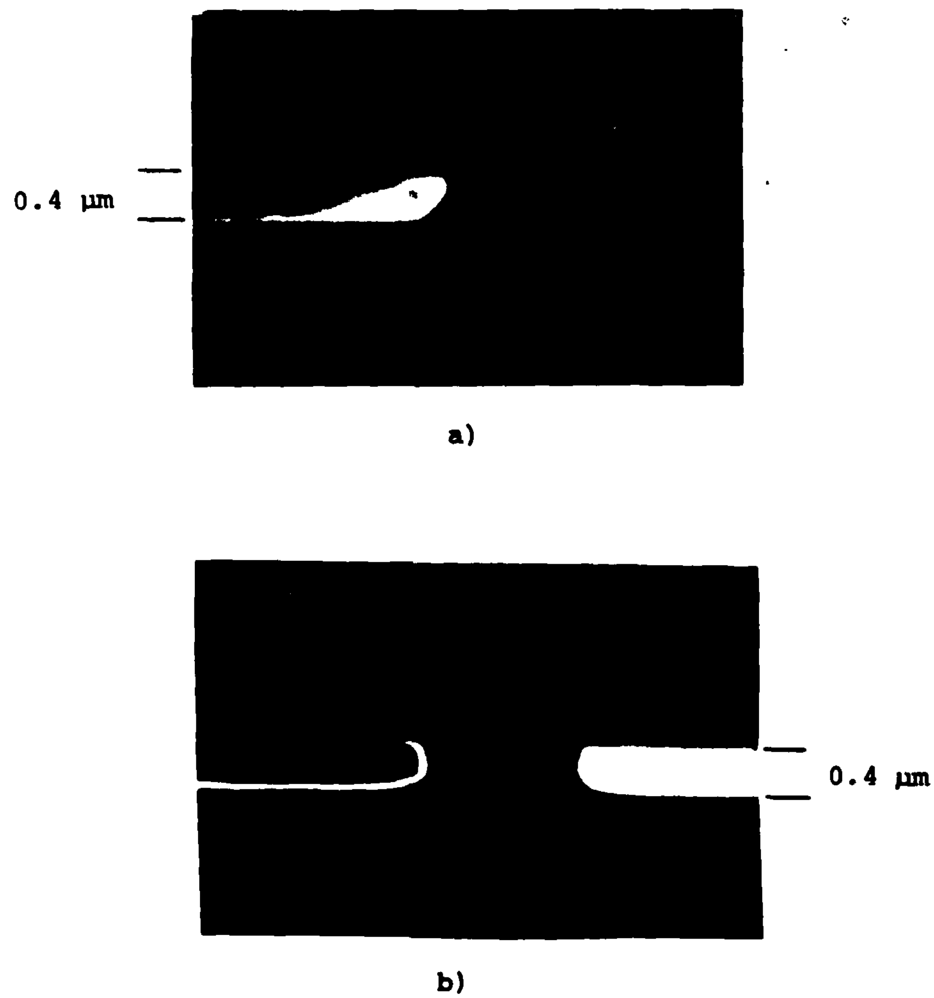


Fig. 4 Ammonium hydroxide/hydrogen peroxide etch profiles in $In_{.53}Ga_{.47}As$:

(a) cross-section for gates parallel to grains.

(b) cross-section for gates perpendicular to grains.

One of the potential problems that JFETs have that MESFETs do not have is the gate contact resistance (which is not to be confused with the resistance associated with resistivity of the gate metal). Since a 1-μm gate 300-μm wide has an area of $3 \times 10^{-6} cm^2$, the specific contact resistance, R_c, must be very small. R_c was measured as follows: First, Zn was diffused into two samples of $In_{.53}Ga_{.47}As$ having $n \approx 2 \times 10^{16} cm^{-3}$. One sample had a 1-hour diffusion at 400°C; the second sample had a 4-hour diffusion, also at 400°C. Source/drain contact pads of varying spacing were then formed by evaporating Au/Zn/Au = 500Å/100Å/500Å (Fig. 5a). These were then annealed for 3 min in H_2 at 300°C. Using the analysis of P. L. Hower et. al,[9] R_c was determined. For the piece diffused 1 hour, $R_c = 0\text{-}1 \times 10^{-6}\ \Omega\text{-cm}^2$, while for the other piece, $R_c = (4 \pm 2) \times 10^{-6}\ \Omega\text{-cm}^2$. The scatter in the data suggest that R_c is probably in the low $10^{-6}\ \Omega\text{-cm}^2$ range. When one of the pieces was re-annealed for 90 sec at 320°C in H_2, R_c increased to $1.2 \times 10^{-5}\ \Omega\text{-cm}^2$. Based on this limited data, it appears that 3 min at 300°C is the preferred contact anneal.

A 1-hour diffusion at 400°C results in a p-n junction about 0.25 μm deep. This depth was obtained by etching the pieces used for the contact resistance measurements until the p-layer was just barely etched, except beneath the contact pads (Fig. 5b). The etching was done in steps using the 25:1 citric acid:hydrogen peroxide etch. Before this p-layer is etched away, the pad-to-pad I-V is nearly ohmic. After it has been etched through, the pad-to-pad I-V is that of a p-n-p diode. For such a diode, there is always one p-n junction that is reverse biased, so leakage currents should be small, assuming that neither p-n junction is shorted by the metal lips of the contact pads. For pads $50 \times 200\ \mu m^2$, the leakage current was as low as 3 nA at 5 volts. Perhaps more important was the observation that most pads had low leakage, usually less than 1 μA at 5V. Hence we obtained the important result that at least for shallow etches, metal can be used as an etch mask and will usually not short out an underlying p-n junction. (However, if the metal lips

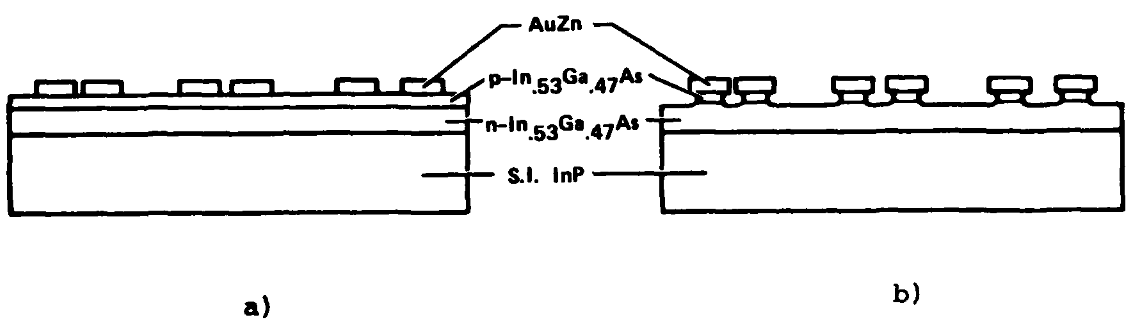


Fig. 5 Cross-section of wafer for contact resistance measurement:

(a) before etch

(b) after p-layer has been etched through.

formed by undercutting are large compared to the metal thickness, it is probable that shorts will occur.)

The specific contact resistance of pure Au contacts to p^+-$In_{.53}Ga_{.47}As$ was also measured. Unannealed contacts on a 0.25-μm thick p-layer formed by a 1-hour diffusion at 400°C had $R_c = 5.6 \times 10^{-4}$ Ω-cm^2. A 90-sec anneal at 320°C in H_2 reduced R_c to 1.4×10^{-4} Ω-cm^2, which is still ~100 times larger than for the best AuZn contacts. Part of the unannealed piece was etched to remove the p-layer, except beneath the contact pads. A subsequent 90-sec anneal at 320°C had little effect on the (small) leakage current of a reverse-biased pad (the other terminal was an ohmic contact to the n-InGaAs layer). However, an additional 90-sec anneal at 350°C in H_2 caused all the diodes to become shorts. Hence the 350°C anneal damaged the junction that was 0.25-μm deep, whereas the 320°C anneal did not. Fortunately, AuZn makes a fairly good ohmic contact, even at lower temperatures (300°C). It is evident, however, that the junction must not be too shallow or it will be degraded by the contact anneal. One FET wafer used a 30-min diffusion at 400°C and had a junction depth of about 1500-2000 Å. Leakage current was a little higher than for the 2500 Å deep junctions and seemed relatively noisy (as seen on a curve tracer). Hence, the minimum junction depth for our process is probably about 1500 Å and should preferably be 2500 Å or larger. Excessively deep junctions should also be avoided in order to more accurately control the channel thickness. Junction depths between 0.25 μm and 0.4 μm are probably best. Junction depth seemed to scale with time (t) more weakly than the expected $t^{1/2}$ dependence; the dependence may be as weak as $t^{1/4}$.

As mentioned above, the source and drain contacts consist of Au/Sn/Au = 100Å/200Å/1000Å. These are annealed along with the gate contacts at 300°C for 3 min in H_2. Higher temperatures cause excessive pitting in the AuSn contacts, and presumably, higher contact resistance. Other work at Varian[10] has indicated that AuSn forms a very low resistance ($\lesssim 10^{-6}$ Ω-cm^2) contact to $In_{1-x}Ga_xAs_yP_{1-y}$ having $E_g \approx 1.0$ eV.

Even lower resistance would be expected for $In_{.53}Ga_{.47}As$, due to the lower bandgap (0.75 eV). Hence the parasitic source and drain resistance will probably be dominated by the channel resistance rather than the contact resistance, for these $In_{.53}Ga_{.47}As$ JFETs.

3.3 JFET Results and Evaluation

To simplify development of the fabrication process described above in Sec. 3.2, we chose to begin with rather lightly doped ($n = 2\text{-}3 \times 10^{16}\ cm^{-3}$) $In_{.53}Ga_{.47}As$, since $10^{17} cm^{-3}$ $In_{.53}Ga_{.47}As$ begins to have avalanche/ tunneling breakdown at only a few volts. Hence the transconductance g_m, which increases as $\sqrt{n}$, is not yet optimized. In the future, dopings in the $7\text{-}10 \times 10^{16} cm^{-3}$ range might be used, which would increase g_m by a factor of ≈ 2. In addition, a gate mask with a gate length of 1.5 μm was used in order to simplify photolithography and potential undercut problems during etching. Now that the process has proven feasible, smaller gates may be used.

Five different FET wafers have been fabricated thus far. All came from a single large wafer grown by MBE, which had an $In_{.53}Ga_{.47}As$ layer with thickness of 0.7 μm and doping of $n = 2\text{-}3 \times 10^{16} cm^{-3}$. All FETs had gate metallizations that were ≈ 1.5 μm long and 300 μm wide.

The source/drain characteristic for one of the more recently fabricated FETs (wafer M71-4) is shown in Fig. 6. This FET, which is typical of most of the FETs on this wafer, has $g_m \approx 20$ mS, $I_{DSS} = 55$ mA, and a pinchoff voltage of $V_p \approx 2.5V$. Values of g_m up to 28 mS were observed on this wafer. The p^+ region is about 0.25 μm deep and was formed by a 1-hour diffusion at 400°C. Gate leakage currents were as low as 20 nA at 2V, but tended to increase for biases above the pinchoff voltage (≈2.5V) (there is no buffer layer). A typical source/gate I-V characteristic for wafer M71-4 is shown in Fig. 7. Note the very low leakage current at reverse biases.

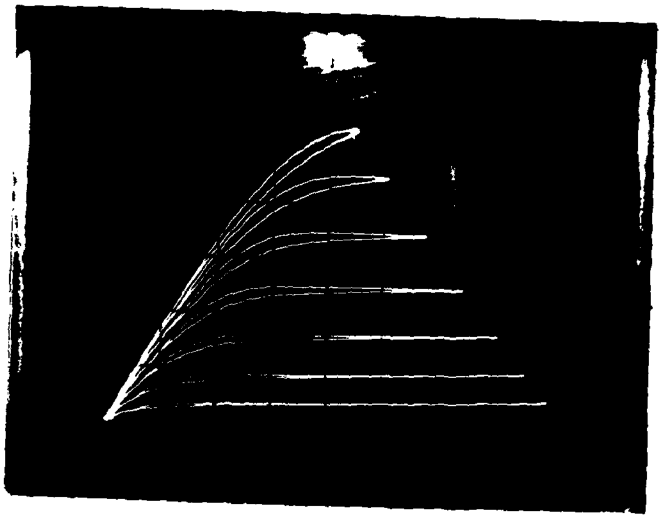


Fig. 6 Typical drain characteristic for sample M71-4.
(0.5 V/div, 10 mA/div, -0.5 V/step)

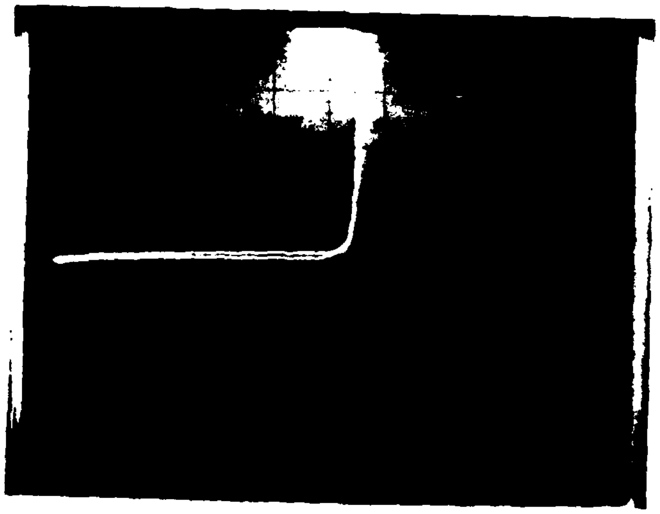


Fig. 7 Gate-source I-V characteristic for sample M71-4. (0.5 V/div, 1 μA/div).

The FET characteristics go through significant changes as the p^+ region away from the gate is etched away; i.e., as the structure of Fig. 2e is changed to the structure of Fig. 2f. We will describe these changes for wafer M71-4. Before the etch, as mentioned earlier, the gate is shorted to the drain through the p^+ layer (Fig. 2e). Typically, gate-drain currents of ~20 mA occur at 1V reverse bias (i.e., negative gate voltage and I_{DSS} is typically ≈ 45 mA. After 60 sec of etching in the citric acid etch (i.e., 25 citric acid (50% by weight):$1H_2O_2$ (30% solution)), part of the p^+ layer is removed. The gate/drain leakage is then ~10 mA at 1V reverse bias and I_{DSS} is still ≈45 mA. After an additional 60 sec etch, the gate/drain leakage becomes <u>typically</u> ~50 μA at ± 1V and I_{DSS} is still ~45 mA. The reduced gate/drain leakage suggests that the remaining p^+-layer is ≲ 100 Å thick. Since the leakage is typically of the same order of magnitude across the whole wafer, it would appear that the etch depth is uniform to within ≈100 Å. At this stage, normal FET characteristics can now be observed; g_m's range up to 28 mS, with 24 mS more common.

After an additional 30-sec etch, gate/drain leakage becomes typically ~10 μA at 1V and g_m is still typically about 24 mS. However, typical I_{DSS} increases to ≈ 55 mA. The increase in I_{DSS} suggests that the p-layer away from the gate metal has been completely removed. Hence the external channel (i.e., away from the gate metal) no longer has a depletion region at the top of the n-layer, and thus can carry more current under saturation conditions; this increases I_{DSS}. An additional 30-sec etch further reduces gate leakage; at 2V reverse bias, leakage current is as low as 20 nA with 100 nA more common. Typical g_m's (at $V_G = 0$) are slightly smaller, about 20 mS, while the largest g_m is 24 mS. Figures 6 and 7 are the FET characteristics observed at this stage of the etching.

All FET wafers went through similar stages as they were being etched. Wafer M71-3 was etched to the same stage as the last stage just described for M71-4. Typical gate leakage current was ~1 μA at 2V, and I_{DSS} was typically ≈ 80 mA. For wafer M71-3, Zn was diffused for only 1/2 hour at 400°C and the junction depth was about 0.15 to 0.2 μm. This diffusion is shallower than for M71-4 (which was diffused for 1 hour at 400°C, resulting in a junction ≈0.25 μm deep). Hence M71-3 has a thicker channel than M71-4, which is consistent with its larger I_{DSS} (80 mA vs 55 mA). Wafer M71-3 was then etched an additional 12 sec. This reduced typical I_{DSS} to 70 mA; typical leakage currents were unchanged. The reduced I_{DSS} occurs because the exterior channel is now thinner than the interior channel (i.e., under the gate metal) due to the extra etching. The leakage currents on this wafer (~1 μA) were significantly higher than on M71-4 and suggest that the junction is a little too shallow to avoid being damaged during the contact anneal. Further etching continues to reduce I_{DSS} and (consequently) causes g_m compression to occur near $V_G = 0$.

It is a significant finding that most FETs on a given wafer _simultaneously_ go through the various stages during etching -- even for 12-sec etch steps. This indicates that the etching is very uniform across the wafer. It would be feasible to etch down to a junction even as deep as 0.4 μm. We might comment that while the uniformity across the wafer is excellent, the etch rate itself seems to vary from day to day, or wafer to wafer, perhaps because the citric acid etch weakens with age or use. Etch rates are in the 10-40 Å/sec range with 20 Å/sec perhaps typical.

We have made measurements that determined upper limits for the gate, source, and drain resistances. We measured the dynamic resistance of the gate-drain junction (R_{GD}) and the gate-source junction (R_{GS}) at a forward current of 50 mA. The better FETs have a spacing between the source and gate metals of about 1.0 μm and a gate-drain separation of about 4.0 μm. Such FETs have R_{GS} = 7Ω and R_{GD} = 11Ω. By stepping the drain current and noticing the voltage shift of the gate-source I-V characteristic, the source resistance (R_S) can be estimated. The better FETs have R_S = 2Ω. The channel thickness after etching is a ≈ 0.4 μm, as determined by the pinchoff voltage, along with the approximately-known doping ($n \sim 2.5 \times 10^{16} cm^{-3}$):

$$a = \sqrt{2\kappa\epsilon_o(V_p + \phi)/ne} \quad ; \qquad (1)$$

a ≈ 0.4 μm is also obtained from the photomicrographs of FETs taken on the scanning electron microscope. For a mobility of 8000 cm^2/V-sec, a channel length of 1.0 μm has a resistance of 2.6 Ω. Since $R_S \approx 2$ Ω was measured, it is evident that the source (or drain) contact resistance must be negligible compared to the resistance of the external channel.

Subtracting R_S from R_{GS} gives an estimate for the upper limit of the gate series resistance under reverse bias conditions of R_G = 5 Ω. This value is an upper limit because:

1) Current under forward bias tends to flow mainly in the edge of the gate near the source. Hence the full gate area is not being utilized under forward bias, with the result that the gate contact resistance is exaggerated;

2) R_{GS} includes a fraction of the internal channel resistance;

3) R_{GS} includes about 1 ohm for the intrinsic resistance of a p-n junction biased to 50 mA (assuming a non-ideality factor of n = 2).

Item (3) alone suggests a better estimate for R_G is $R_G \approx 4$ Ω. Part of R_G is due to the finite resistivity of the gate metal, ρ_G. This resistance contribution is[11]

$$R_{G,MET} = \frac{\rho_G z^2}{3L_G hZ} \qquad (2)$$

Here L_G is the gate metal "length" ($\approx$ 1.5 μm), z is the unit gate width (150 μm), and h is the height of the AuZn gate metal ($\approx$ 0.3 μm). Taking $\rho_G = 5 \times 10^{-6}$ Ω-cm for AuZn (which is also the value measured for aluminum gates[11]), results in $R_{G,MET} = 3$ Ω. Smaller values could be obtained by using thicker gate metals. With $R_G \approx 4$ Ω and $R_{G,MET} = 3$ Ω, there is then only about 1 ohm left for the contact resistance of the gate. The specific contact resistance would then be $\approx 4 \times 10^{-6}$ Ω-cm, which is consistent with the more direct measurements described in Sec. 3.2.

In summary, the JFET parasitic resistances that effect noise and gain are small: Source and drain contact resistances are negligible, gate contact resistance is small (in the low 10^{-6} Ω-cm^2 range), and the resistivity of the AuZn gate metal is low and comparable to aluminum.

We now discuss the magnitudes of the g_m values that have been obtained. To a first approximation, there is velocity saturated current flow under the entire gate. For this case, g_m is theoretically given by[1,12]

$$g_m = Z\, v_s \sqrt{\kappa\varepsilon_o ne/2(-V_G + \phi)} \quad , \qquad (3)$$

where v_s is the saturated drift velocity and κ is the relative dielectric constant ($\approx$12.5); V_G is the gate voltage relative to the source, and ϕ is the built-in voltage ($\approx$0.6V). For $V_G = 0$, $\phi = 0.6$V, $\kappa = 12.5$, n $= 2.5 \times 10^{16}$cm^{-3} and Z = 300 μm (as for our FETs), and for v_s the same as for GaAs (1.3×10^7 cm/sec), Eq. (3) gives

$$g_m\,(V_G = 0) = 24 \text{ mS} \quad . \qquad (4)$$

Observed values of g_m at $V_G = 0$ ranged up to 28 mS with 20-24 mS more typical. Internal values of g_m are expected to be larger by the factor of $(1 - g_m R_s)^{-1}$; this factor usually represents only a 5-10% enlargement. Hence at $V_G = 0$, these JFETs appear to have g_m's only slightly larger at best, than corresponding GaAs FETs would have. However, at finite gate biases, ($V_G < 0$), significant improvement occurs.

For example, when $V_G = -1.8V$, Eq. (3) predicts that g_m should be half of the value for $V_g = 0$. Instead, we observe that g_m's are only slightly smaller at $V_G = -1.8V$ than at $V_G = 0$. For example, Fig. 6 shows a JFET with $g_m \approx 20$ mS at $V_G = 0$ and $g_m = 18$ mS at $V_G = -1.8V$. Corresponding values of internal g_m's are about 21-22 mS and 19-20 mS. A value of only 12 mS would be expected at $V_G = -1.8V$ if v_s were the same in $In_{.53}Ga_{.47}As$ as in GaAs. Hence $In_{.53}Ga_{.47}As$ offers a substantial improvement over GaAs. Earlier work in this program[1-3] has indicated that v_s can be twice as large in $In_{.53}Ga_{.47}As$ as in GaAs, thus leading to a predicted increase in g_m by as much as a factor of two.

Evidently there is some g_m compression occurring toward $V_G = 0$ in these JFETs. It is possible that this is associated with the diffusion process. H. Ando et al.[13] have studied Zn (and Cd) ampoule-type diffusions in InP and have concluded that there is a compensated region extending beyond the p-n junction depth. They speculate that this region is caused by deep levels associated with neutral Zn (or Cd). This is perhaps not surprising since the solid solubility of substitutional Zn in InP is about $2 \times 10^{18} cm^{-3}$, yet surface concentrations are in the 10^{19}-$10^{20} cm^{-3}$ range. The situation in $In_{.53}Ga_{.47}As$ is probably similar to InP, although $In_{.53}Ga_{.47}As$ has a higher solubility for Zn. This compensated region may be the cause of the looping observed in the FET characteristics (Fig. 6); lack of a buffer layer may also contribute. It would be interesting to form the p^+ region by ion implantation rather than diffusion, thereby reducing peak concentrations to below solid-solubility. (It is only the Zn in excess of the solid-solubility of substitutional Zn that diffuses rapidly and causes the compensated region ahead of the p-n junction.) Shallow (0.4-μm deep) p^+ junctions formed by Mg or Be implants have already been successfully used at Varian to consistently make high-quality InP impatt diodes.

Finally, we should point out that the best noise performance is usually obtained near ~20% of I_{DSS}. This is rather far from the g_m compression region near $V_G = 0$. Hence, these diffused $In_{.53}Ga_{.47}As$ JFETs are likely to provide performance superior to GaAs FETs, even at the present level of development. Rf testing is obviously important and is planned for future more optimized FETs having shorter gates and higher doping (~9 x $10^{16}cm^{-3}$).

3.4 Conclusions and Recommendations

We have demonstrated the feasibility of fabricating $In_{.53}Ga_{.47}As$ JFETs superior to GaAs MESFETs. The major problems have been solved and the remaining problems are mainly of a process-optimization nature. FETs superior to GaAs MESFETs are expected.

The most important areas for future work, we feel, are:

1) optimizing JFETs by using higher dopings (~9 x $10^{16}cm^{-3}$), and smaller gates (~0.5 μm).

2) RF testing of optimized JFETs for gain and noise figure.

3) Testing Mg or Be ion implantation as an alternative to Zn diffusion to try to eliminate g_m compression near $V_G = 0$.

4) Optimization of contacts. Other metals or annealing conditions may lead to lower contact resistance and/or might allow shallower p-n junctions.

5) Development of a buffer layer. High resistivity InAlAs layers lattice matched to InP are within easy reach of present MBE technology. High-resistivity $In_{.53}Ga_{.47}As$ layers may also be possible. Further into the future, semi-insulating InP layers might be possible by MBE.

6) Test LPE-grown $In_{.53}Ga_{.47}As$ and compare to MBE material. Since ~0.7-μm thick layers are acceptable, LPE growth is feasible.

Finally, it should be noted that in certain applications JFETs -- even GaAs JFETs -- may be desirable. GaAs JFETs have been fabricated[14] for logic applications to take advantage of the higher built-in voltage of the p-n junction, which assures a larger noise margin in logic operation. Another application in which JFETs would be preferred is the recently-demonstrated pin-FET optical receiver.[15] Gate leakage currents larger than ≈100 nA degrade sensitivity in this application. To retain < 100 nA leakage up to an operating temperature of 70°C, JFETs rather than MESFETs will be required. Lastly, if JFETs are less prone to 1/f noise than MESFETs, then such FETs will find application in more lower frequency circuits where bipolars are presently preferred.

4. REFERENCES

1. S. Bandy, T. Boyle, R. Fulks, S. Hyder, C. Nishimoto and T. Yep, Interim Tech. Report No. 1: "Research on InGaAs FETs," sponsored by Office of Naval Research Contract N00014-78-C-0380, September 1979.

2. S. Bandy, T. Boyle, R. Fulks, S. Hyder, C. Nishimoto and T. Yep, Interim Tech. Report No. 2: "Research on InGaAs FETs," sponsored by Office of Naval Research Contract N00014-78-C-0380, September 1980.

3. S. Bandy, C. Nishimoto, S. Hyder and C. Hooper, Appl. Phys. Lett. 38, 817 (1981).

4. J. Degani, R. F. Leheny, R. E. Nahory, J. P. Heritage, Appl. Phys. Lett. 39, 569 (1981).

5. R. Yeats, K. Von Dessonneck, SPIE Vol. 272, High-Speed Photodetectors, 22 (1981).

6. R. Yeats, unpublished.

7. N. Susa, Y. Yamauchi, H. Ando and H. Kanbe, IEEE Electron Device Letts. EDL-1, 55 (1980).

8. M. Otsubo, T. Oda, H. Kumabe, H. Miki, J. Electrochem. Soc. 123, 676 (1976).

9. P. L. Hower, W. W. Hooper, B. R. Cairns, R. D. Fairman and D. A. Tremere, Semiconductors and Semimetals 7A, 147 (1971).

10. Y. G. Chai, unpublished.

11. H. Fukui, Bell Sys. Tech. J. 58, 771 (1979).

12. R. A. Pucel, H. A. Haus and H. Statz, Advances in Electronics and Electron Physics 38, 195 (1975).

13. H. Ando, N. Susa, H. Kanbe, Jap. J. Appl. Phys. 20, L197 (1981).

14. M. Dohsen, J. Kasahara, Y. Kato and N. Watanabe, IEEE Electron Device Letts. EDL-2, 157 (1981).

15. D. R. Smith, R. C. Hooper, H. Ahmad, D. Jenkins, A. W. Mabbitt, and R. Nicklin, Electron. Lett. 16, 69 (1980).

APPENDIX A

AN ALTERNATIVE, BUT UNSUCCESSFUL, JFET FABRICATION SCHEME

An alternative scheme for fabricating $In_{.53}Ga_{.47}As$ JFETs was also investigated. The scheme involves using the gate metal (which contains Zn) as a Zn-diffusion source during a long "contact anneal" step. If successful, this scheme would lead to a JFET fabrication process that is similar to the familiar MESFET process. Unfortunately, this technique failed to produce p-n junctions with low enough leakage current.

The metal systems that were tested were:

1) Au/Zn/Au = 500/100/500 Å.

2) TiW/Au/Zn/Au = 1000/1200/150/400 Å.

3) Ti/Pt/Au/Zn/Au = 700/500/600/150/400 Å.

4) Pt/Au/Zn/Au = 100/600/150/400 Å.

For the first metal system, the metals were e-beam evaporated. For the last three metal systems, the first layers were deposited by sputtering, while the remaining metal was an e-beam evaporation of Au/Zn/Au = 200/150/400 Å. There were two types of substrates upon which these metals were deposited:

1) a lattice-matched layer of LPE-grown $In_{.53}Ga_{.47}As$ having $n \approx 1 \times 10^{16}$ cm^{-3};

2) a polished wafer of bulk InP having $n \approx 4 \times 10^{17} cm^{-3}$.

The metals were patterned by standard photolithographic liftoff techniques into dots having various diameters ranging between 1 mil and 6 mils. A variety of annealing (diffusing) times from 1 h to 70 h at temperatures of 240°C to 400°C were investigated. The lowest leakage occurred for the Au/Zn/Au system when it was annealed for 14h at 300°C in hydrogen. Typical 2-mil diameter $In_{.53}Ga_{.47}As$ diodes had 70-μA leakage at 1V reverse bias; (40 μA was the best value). Comparison with different size diodes indicated that the leakage current was area rather than perimeter dependent. (The second terminal in these measurements was an ohmic contact to the n-layer at the edge of the sample.) In the forward-bias direction, these diodes had a voltage of only 0.1-0.2V at 0.5 mA. (Values of ~0.4V at 0.5 mA are typical of good $In_{.53}Ga_{.47}As$ p-n junctions.) Attempts to C-V profile these diodes failed due to the large leakage current.

Worse results were obtained for the other metal systems (#2,3, and 4). One-hour anneals in hydrogen were made at temperatures of 300°C, 350°C, and 400°C (using a separate piece of the wafer for each temperature). There was no sign of surface decomposition under high magnification (1000X) for either the InP or the $In_{.53}Ga_{.47}As$ substrates. All these samples had a similar order of magnitude leakage current, which was approximately 1 mA at 1-2V for 1-mil diameter dots. There was slight asymmetry in the I-V characteristics, indicating a small degree of rectification. Metal system #4 (Pt-base) was the most rectifying, followed in order by #3 (Ti-base) and #2 (TiW-base).

Surprisingly, there was no change in appearance of the TiW-based system (#2) after being annealed for 1h at 400°C, even under high magnification (1000X). The other metal systems tested (#4 & #3) were affected by 1 hour at 400°C, but not by 1 hour at 300°C. At intermediate temperatures, metal dots on the InP substrate were affected more than the dots on the $In_{.53}Ga_{.47}As$ substrate, presumably because of relatively rapid P diffusion into the metals.

DISTRIBUTION LIST - FINAL REPORT
CONTRACT N00014-78-C-0380

Code 414 Office of Naval Research Arlington, VA 22217	4
Naval Research Laboratory 4555 Overlook Avenue, S.W. Washington, DC 20375 Code 6811 6850	 1 1
Defense Documentation Center Building 5, Cameron Station Alexandria, VA 22314	12
Dr. Y. S. Park AFWAL/DHR Building 450 Wright-Patterson AFB Ohio 45433	1
ERADCOM DELET-M Fort Monmouth, NJ 07703	1
Texas Instruments Central Research Lab M.S. 134 13500 North Central Expressway Dallas, TX 75265 Attn: Dr. W. Wisseman	1
Dr. R. M. Malbon/M.S. 1C Avantek, Inc. 3175 Bowers Avenue Santa Clara, CA 94304	1
Mr. R. Bierig Raytheon Company 28 Seyon Street Waltham, MA 02154	1
Dr. R. Bell, K-101 Varian Associates, Inc. 611 Hansen Way Palo Alto, CA 94304	1
Dr. Mike Driver Westinghouse Research and Development Center Beulah Road Pittsburgh, PA 15235	1
Dr. D. Richard Decker Rockwell International Science Center P.O. Box 1085 Thousand Oaks, CA 91360	1
Dr. C. Krumn Hughes Research Laboratory 3011 Malibu Canyon Road Malibu, CA 90265	1
Mr. Lothar Wandinger ECOM/AMSEL/TL/IJ Fort Monmouth, NJ 07003	1
Dr. Harry Wieder Naval Ocean Systems Center Code 922 271 Catalina Blvd. San Diego, CA 92152	1
Dr. William Lindley MIT Lincoln Laboratory F124 A, P.O. Box 73 Lexington, MA 02173	1
Commander U.S. Army Electronics Command V. Gelnovatch (DRSEL-TL-IC) Fort Monmouth, NJ 07703	1
RCA Microwave Technology Center Dr. F. Sterzer Princeton, NJ 08540	1

Hewlett-Packard Corporation 1
Dr. Robert Archer
1501 Page Road
Palo Alto, CA 94306

Watkins-Johnson Company 1
E.J. Crescenzi, Jr./
K. Niclas
3333 Hillview Avenue
Stanford Industrial Park
Palo Alto, CA 94304

Commandant 1
Marine Corps
Scientific Advisor (Code AX)
Washington, DC 20380

Communications Transistor Corp. 1
Dr. W. Weisenberger
301 Industrial Way
San Carlos, CA 94070

Microwave Associates 1
Northwest Industrial Park
Drs. F.A. Brand/J. Saloom
Burlington, MA 01803

Commander, AFAL 1
AFWAL/AADM
Dr. Don Rees
Wright-Patterson AFB, Ohio 45433

Professor Walter Ku 1
Phillips Hall
Cornell University
Ithaca, New York 14853

Commander 1
Harry Diamond Laboratories
Mr. Horst W.A. Gerlach
800 Powder Mill Road
Adelphia, MD 20783

Advisory Group on Electron 1
Devices
201 Varick Street, 11th Floor
New York, NY 10014

Dr. Ken Weller 1
MS/1414
TRW Systems
One Space Park
Redondo Beach, CA 90278

Professor L. Eastman 1
Phillips Hall
Cornell University
Ithaca, NY 14853

Professor Hauser and 1
Littlejohn
Department of Electrical Engineering
North Carolina State University
Raleigh, NC 27607

Professor J. Beyer 1
Department of Electrical and
Computer Engineering
University of Wisconsin
Madison, WI 53706

Professor Rosenbaum and Wolfe 1
Semiconductor Research Laboratory
Washington University
St. Louis, MO 63130

W. H. Perkins 1
Electronics Lab 3-115/B4
General Electric Company
P.O. Box 4840
Syracuse, NY 13221

Bryan Hill 1
AFWAL/AADE
Wright-Patterson AFB, Ohio 45433

H. Willing/Radar Directorate 1
BMD - Advanced Technical Center
P.O. Box 1500
Huntsville, Alabama 35807

ATE

LME

-8